

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|-------|---|------------------------------|------------------|---------|------------------|
| S32 | 51 | ("4527145" "5099477").PN. OR ("5448715").URPN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/11/27 17:10 |
| S34 | 57 | S33 same (memory adj2 controller) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:15 |
| S33 | 7648 | (clock domain) near3 (translat\$3 cross\$3) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:15 |
| S36 | 3 | S34 and S35 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:27 |
| S35 | 9511 | \$2ram near3 ((pre adj charg\$3) precharg\$3 refresh\$3) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:27 |
| S39 | 23 | S37 same (clock near3 (cross\$3 translat\$3)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:33 |
| S38 | 217 | S37 and (clock near3 (cross\$3 translat\$3)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:33 |
| S37 | 33167 | (memory \$2ram) near3 ((pre adj charg\$3) precharg\$3 refresh\$3 clos\$3) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/11/27 17:33 |
| L4 | 11 | ((cpu processor) near2 clock) near3 (faster slower) with ((memory ram) near2 clock) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 13:52 |
| L5 | 27 | precharge with close with refresh | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 14:11 |
| L8 | 54 | 6 with refresh\$3 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 14:12 |
| L7 | 294 | 6 with memory | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 14:12 |
| L6 | 1492 | (precharg\$3 pre-charge\$3) near6 clos\$3 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 14:12 |
| L10 | 184 | dma near5 delay | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:36 |
| L9 | 13 | 8 same (memory near3 (controller interface)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:36 |

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| L12 | 247 | dma near3 delay\$3 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:41 |
| L11 | 7 | 10 with ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:41 |
| L13 | 4 | 12 near6 ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:49 |
| L16 | 476 | dma near3 ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:50 |
| L15 | 0 | 12 same "not ready" | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:50 |
| L14 | 0 | 12 with "not ready" | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:50 |
| L17 | 10 | 16 with delay\$3 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:52 |
| L18 | 22 | dma near3 ready near5 (flag bit) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:53 |
| L19 | 7 | 18 with wait\$3 | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 15:56 |
| L21 | 63354 | memory adj (controller interface) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:00 |
| L22 | 7 | 21 and (dma near3 (wait\$3 delay\$3) near3 ready) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:05 |
| L23 | 4 | dma with (completion adj bit) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:06 |
| L24 | 1836 | dma adj engine | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:16 |
| L20 | 14 | dma near3 wait\$3 near3 ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:16 |
| L25 | 42 | 24 near5 (delay\$3 wait\$3) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:17 |

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| L27 | 707 | dma with sdram | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:20 |
| L26 | 22 | dma near3 ready near5 (registar flag bit) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:20 |
| L28 | 7 | dma near3 (wait\$3 ready delay\$3) with sdram | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:21 |
| L30 | 120 | 29 and (dma near6 (ready wait\$3 delay\$3)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:23 |
| L33 | 2 | 32 and dma | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/12/08 16:26 |
| L32 | 11 | ("3728692" "4348725" "5136710" "5210872" "5371887" "5600837" "5630130" "5761522" "5799182" "5867704" "6085218").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/12/08 16:26 |
| L34 | 19128 | dma near3 (ram dram sdram memory) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:27 |
| L31 | 5 | 29 and (dma near6 (ready wait\$3 delay\$3) with (status register flag bit)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:27 |
| L29 | 309 | dma near3 sdram | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:27 |
| L36 | 37246 | 34 sae (dma near6 (ready wait\$3 delay\$3) with (status register flag bit)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:28 |
| L35 | 391 | 34 and (dma near6 (ready wait\$3 delay\$3) with (status register flag bit)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:28 |
| L39 | 2652 | 38 with dma | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:37 |
| L38 | 63880 | (memory sdram) adj (controller interface) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:37 |
| L37 | 56 | 34 same (dma near6 (ready wait\$3 delay\$3) with (status register flag bit)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:37 |
| L40 | 1041 | 38 with (dma adj (controller engine)) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 16:38 |

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| L41 | 31 | 40 and (dma near3 ready) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:02 |
| L42 | 10234 | dma adj (engine controller) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:03 |
| L43 | 15 | 42 same (dma near6 (wait\$3 delay\$3) near3 ready) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:16 |
| L46 | 113 | dma near3 status near3 bit | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:17 |
| L44 | 345 | dma near3 (status ready) near3 (register bit) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:17 |
| L50 | 7 | 49 with ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:18 |
| L49 | 338 | dma near3 status near3 (register bit flag) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:18 |
| L48 | 0 | 47 with ready | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:18 |
| L47 | 25 | dma adj status near3 (bit flag) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:18 |
| L45 | 355 | dma near3 (status ready) near3 (register bit flag) | US-PGPUB; USPAT; EPO | OR | OFF | 2006/12/08 17:18 |